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**HARNESSES**  
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November 17, 2004

10/050 745

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Re: U.S. Patent No. 6,785,106 *B2*  
Issued: August 31, 2004  
Title: Integrated Circuit Device  
Inventor: Junichi Nagata  
Docket No. 4041P-000033

**Certificate**  
**NOV 30 2004**  
**of Correction**

Sir:

We have reviewed the above-indicated patent and have found an error which requires a Certificate of Correction.

Title Page, Title: (Application, page 1, line 1), "Integrate" should be --Integrated--; and

Col. 1, line 1, (Application, page 1, line 1), "Integrate" should be --Integrated--.

Enclosed herewith is an original and a carbon copy of the Patent and Trademark Office Certificate of Correction form which we request be approved for the above-identified patent. Please note that the above is a Patent Office error:

Please consider this as authorization to charge our Deposit Account No. 08-0750 for any fee which may be due should it be determined that the error is Applicants' fault. A duplicate copy of this letter is enclosed.

Respectfully submitted,

H. Keith Miller, Esq.  
Reg. No. 22,484

HKM/rf  
Attachments

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6 DEC 2004

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(Also Form PTO-1050)

## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 6,785,106 *B2*  
DATED : August 31, 2004  
INVENTOR(S) : Junichi Nagata

Page 1 of 1

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MAILING ADDRESS OF SENDER:

HARNESS, DICKEY & PIERCE, P.L.C.  
P.O. BOX 828  
BLOOMFIELD HILLS, MI 48303

6,785,106 *B2*  
PATENT NO. \_\_\_\_\_

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